# Exam 2024

Indholdsfortegnelse

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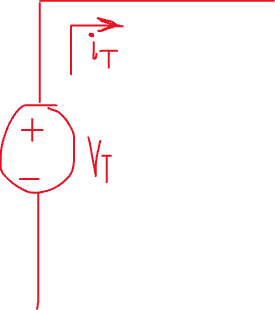
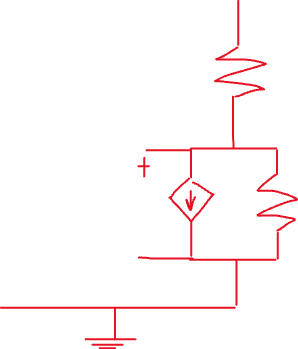
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## Question 1. Find the looking resistance . Assume and current source is a biased Nmos ( Diode koblinger )

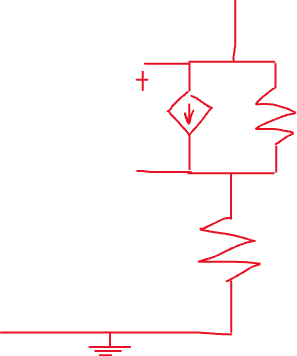
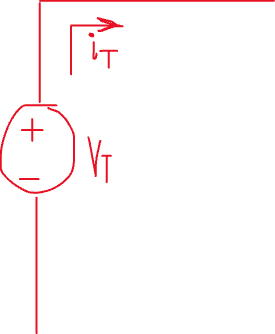
Et billede, der indeholder tekst, skærmbillede, Font/skrifttype, diagram

Automatisk genereret beskrivelse



For   
   
This equation can be simplified to.   
   
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As the the current source is driven by the a nmos  
for small signal Rin analysis, the input of that will  
be set to ground. Only the internal resistance will   
stay. Again as before I see a resistor in series with   
a diode connected nmos.  
Therfore   
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## Et billede, der indeholder diagram, Font/skrifttype, hvid, linje/række Automatisk genereret beskrivelseQuestion 1. What are the possible regions for and ? What are the reasons for these possibilities? Prove it using equations. ( Cascode kobling



Et billede, der indeholder tekst, skærmbillede, Font/skrifttype, linje/række

Automatisk genereret beskrivelse  
   
Can the circuit fullfill that?.   
For that to happen, no voltage should be lost across the M2 transistor. , which means it’s in cutoff so zero current, or close to, runs through the circuit.



What about saturation for the M2 and linear for the second?   
   
   
The drain source voltage should be satisfied with being in linear as long as:

, will for Vthn being positive, which it for my knowledge, always is. So the drains source voltage is met.  
   
And this should ensured, as long as VD is about threshold voltage. As both gates need to have atleast threshold voltage, that’s the minimum requirement  
=====================================  
For   
M1 in the linear region, should be fullfilled, and   
M2 in the saturation region as well.   
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## Question 2. Find the gain and the in the figure below. Assume . What function might the circuit perform based on the gain equation?

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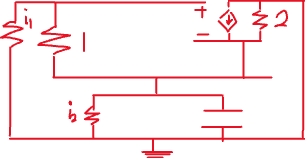
Automatisk genereret beskrivelse

I’ll be finding the small signal gain for this circuit.   
Assuming that the current sources isn’t of mosfets. Otherwise I would have added their resistances, . Nah that might be wrong, as the CL would then never be used, as vout would be shorted.

# New approach. I assume every current source, to be of biasing nmoses



‘’’



Så I have   
, let me find this.

And is the respective impedance for that path.

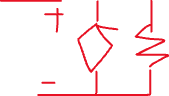
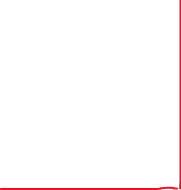
I need substitution for the last one.   
   
   
   
  
   
   
   
   
  
So the output impedance is:   
  
   
=================================================  
   
=================================================

This is calculated wrong, as I’ve drawn the pmos as a nmos equivalent. I must have to recalculate it, but it won’t be much different.

To find the gain I then need the transconductance.

Et billede, der indeholder diagram, Font/skrifttype, linje/række

Automatisk genereret beskrivelseNow the vout is shorted.



## Question 3. If the ”auxiliary current sources”, M5 and M6, carry 80% of the drain current of M1 and M2 ( Assume . ( Diode, biasing, differential & common mode, 20 )

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1. Find differential & common mode gain
2. Find the poles in differential mode

## Question 4. Figure below shows a cascode stage ( Assume ). ( Cascode kobling, dc gain, mos capacitors, transfer function. 40 )

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1. Calculate the DC gain.

From example 6.7 in the book I find a similar circuit, but here with a biasing transistor for a current source.

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Automatisk genereret beskrivelseEt billede, der indeholder diagram, linje/række, Font/skrifttype

Automatisk genereret beskrivelseHere they’ve found that   
Et billede, der indeholder tekst, Font/skrifttype, linje/række, håndskrift

Automatisk genereret beskrivelse   
And their output acts as my source to the biased transistor.

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Automatisk genereret beskrivelseMaking the assumption, that for a bias transistor, I shouldn’t care about the capacitors, as they will acts as open circuits.   
Thereby the upper circuit can be described by a common gate configuration. It’s Rs is set to 0.   
It’s gain is

And as

------ Correcting my previous assumption ------

That I could just use the examples calculation straight ahead. That’s not true if , so let me adjust it a little.   
It was made using miller effect, and simplified from this circuit.   
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As for every RD was supposed to be in parallel with ro and therefore. RD was further simplified to be 0. As they were in parallel, ro just replaces RD in my equation.

The DC gain is then:   
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1. Et billede, der indeholder diagram, Font/skrifttype, håndskrift, tekst

   Automatisk genereret beskrivelseSketch the high-frequency components (capacitors) in the figure.

Did I already do that?   
I made the assumption for the bias transistor to have no transistor attached to it, as it’s at DC only. Now it might have some small mistakes in it. But it might be okay for some purposes. Now this was my sketch then:

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Automatisk genereret beskrivelse

1. Compute the

I already did that.

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